A Novel Approach for Introducing Digital Systems Labs

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Abstract

Traditional digital system courses commonly spend significant time at the start of each semester introducing binary number systems prior to addressing combinational logic networks. While this helps place logic operators in context, it can delays circuit-based labs. When this delay is combined with academic holidays, the first lab using Integrated Circuits can be pushed out until the forth week of a semester. This paper will outline that with a slight change in course sequencing, it is possible to start students off on bit level digital logic circuits and then progress to the encoding of data via the binary numbering system. This allows students to immediately start working with integrated circuits after just one lecture, thus enabling lab sections to utilize the first week of a course.

Introduction

Digital System courses have a long history in Electrical, Electronic, and Computer Engineering curriculums. Its existence in some form can be found in all programs nationwide. Countless textbooks[1,2], lecture packets, and labs have been written. In these courses, instructors seek to educate students in the fundamental concepts of Boolean logic/gates as well as varying numbering systems before proceeding on to other topics.

Grand Valley State University (GVSU) traditional has followed the standard procedure of;
1. Introduction to the digital world.
2. Binary number systems.
3. Other number systems such as Hexadecimal and Octal.

Then once students have been taught how to represent information via ones and zeros, educators transition into Boolean logic followed by the increasing complexity of combinational logic and sequential systems. This sequence is helpful in grouping circuit and non-circuit related topics together. But it also delays the use of logic gates in the accompanying laboratory as students are ill prepared. Two common solutions are to either dedicate lab time to lecturing students on Boolean logic or use the time to introduce electronic test equipment. Both options are viable alternatives, the first allows for "virtual" time to be added to the lectures so more advanced topics can be covered later in the semester, while the latter is extremely help for students that have never used an electronics lab.

The challenge however is introduced when the semester sequence is overlaid on the academic calendar. In that both Fall and Winter semesters often have a holiday within the second or third week of classes. This delays the introduction of Combinational Logic Networks (CLNs) in a laboratory setting until well into the forth week, see Table 1. In order maintain the overall

| | Late Holiday | | Early Holiday | |
Week	Lecture	Lab	Lecture	Lab
1	Introduction Unsigned Number Representation	Digital Tools - Part I (Short Lab)	Introduction Unsigned Number Representation	Digital Tools - Part I (Short Lab)
2	Signed Number Representation Logic Functions	Digital Tools – Part II (Short Lab)	**NO CLASS** Signed Number Representation	**No Lab Due to Holiday**
3	**NO CLASS** Boolean Algebra	**No Lab Due to Holiday**	Logic Functions Boolean Algebra	Digital Tools – Part II (Short Lab)
4	Sum Of Product Equations Karnaugh Maps	Combinational Network (Very Long Lab)	Sum Of Product Equations Karnaugh Maps	Combinational Network (Very Long Lab)
5	Sequential Networks/Review **Exam #1**	Combinational Logic Design	Sequential Networks/Review **Exam #1**	Combinational Logic Design

Table 1: The combination of both a holiday and addressing number representations prior to logic systems delays the combinational logic network lab until the forth week of the semester.

course objectives, instructors then have to cram breadboard construction techniques, multiple Integrated Circuit (IC) systems, and Xilinx (a Computer Aided Design tool, CAD) into just one lab. In the past, this lab has run long and commonly delays the start of the following labs as students are unable to compete all required tasks. In addition students quickly get frustrated with the idiosyncrasies of the CAD package and begin to dislike all labs that utilize it. This problem is compounded by the fact that all engineering students at GVSU are required to take this course, and for many this is their first introduction to operation and design of electrical/electronic systems. Some students have even been heard saying, "I am glad I am not an EE (Electrical Engineering) major."[3]

Proposed Changes
In order to increase interest in digital systems and the EE program at large, one solution currently under experimentation is the shifting of lecture topics. The proposed sequence is based on the fact that logic networks utilize a bit level signal as opposed to a word level signal (a composition of multiple bits). This allows for the disjointing of Boolean algebra from binary numbers. Students are introduced to logic functions directly. Examples of home lighting networks, which all students are familiar with, allow for the connection of the new topics: AND, OR, NAND, NOR, and XOR gates. Once students are taught about bit level operations and simple CLN's, they are introduced to data encoding via different number systems. Students are then able to link the need for the binary number system with a series of CLNs. Some authors like Brown and Vranesic are utilizing this sequence[4], but with a significant focus on Verilog or VHDL. These additional topics, while helpful for EE's, can often intimidate the non-EE majors at GVSU.

This minor shift in topic sequence, creates student that are ready to use basic IC's by the end of week 1. This allows for the combining of GVSU's previous Digital Tool – parts I and II into a

| | Late Holiday | | Early Holiday | |
Week	Lecture	Lab	Lecture	Lab
1	Introduction Logic Functions	Digital Tools	Introduction Logic Functions	Digital Tools
2	Boolean Algebra Sum Of Product Equations	Combinational Network - Part I	**NO CLASS** Boolean Algebra	**No Lab Due to Holiday**
3	**NO CLASS** Karnaugh Maps	**No Lab Due to Holiday**	**Sum Of Product Equations** Karnaugh Maps	Combinational Network - Part I
4	Unsigned Number Representation Signed Number Representation	Combinational Network - Part II	Unsigned Number Representation Signed Number Representation	Combinational Network - Part II
5	Sequential Networks/Review **Exam #1**	Combinational Logic Design	Sequential Networks/Review **Exam #1**	Combinational Logic Design

Table 2: Both the late and early holiday shifted sequence. Note that by shifting the sequence of topics it is possible to introduce students to the construction of combinational networks, in a friendlier environment, by the end of week 3.

single lab, see Table 2. The lengthy Combinational Network lab can then be expanded into two parts, one that focuses on breadboard proto-typing construction and one that only addresses Xilinix. Even with an academic holiday, by the 3rd week of class, students are well on their way to designing and implementing CLN's.

Labs
The first three GVSU labs started out with the following Objectives:
Lab 1 Objectives:
a. Learn how to use a power supply to power digital circuits.
b. Learn how to use a DMM and logic probe to measure logic levels.
c. To use a C compiler IDE and refresh the students C programming skills.
Lab 2 Objectives:
a. Learn how to use a breadboard to construct digital circuits.
b. Learn how to create a digital circuit and simulation in Xilinx ISE.
Lab 3 Objectives:
a. Investigate how combinational logic networks can be used to perform useful functions.
b. Practice working with breadboard circuits.
c. Expand working knowledge of Xilinx.
Each objective in the first two labs was addressed in a separate section, with Lab 1b introducing students to the operation of a logic probe on a variable power supply, while Lab 2a expanded the application of logic probes to a single IC/gate circuit. The third lab prompted students through the design and construction of a full two-bit adder and the design and simulation of a five-bit ripple carry adder. The straight forwardness of the first two labs allowed student to finish them in about two hours, while the complexity of the third lab often took students 4+ hours. The additional time associated with Lab 3, was either made up outside of class as a "homework assignment" or tacked on to the following weeks lab.

With the proposed modification in lecture sequence, students should have a fundamental knowledge of logic gates by the end of the first week. This allows for the combining of Lab 1 and 2 objectives. The new single Digital Tools can be shorted to less then three hours by moving the C programming review objective to a lecture homework assignment. The previous Lab 3 can then be divided into a breadboard based lab, Combinational Networks – Part I that addresses objectives 3a and 3b, and a simulation focused lab, Combinational Networks – Part II that addresses objectives 3a and 3c (compare Table 1 and 2). This allows for additional Xilinx training that can cut down on some of the frustration of the following labs. In addition, the delay of the five bit ripple carry adder allows it to sync nicely with the number system lectures. This reinforces the use of bits and arrays of CLNs to represent binary words/data.

Conclusion

A re-sequencing of GVSU's Digital Systems course was presented. The addressing of logic gates and bit-wise manipulation prior to number systems allows lab topics to be advanced. While this is the first semester of trying this new sequence, student feedback has been positive. There has been a remarkable decrease in frustration associated with Xilinx and there has been a slight uptick in the number of students interested in switching their major to Electrical/Computer Engineering.

Bibliography

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